

**What the invention claimed is:**

1. A programmable logic analyzer data analyzing method comprising the step of controlling a control circuit to fetch waveform data from the test sample and to store fetched waveform data in a memory, the step of controlling said control circuit to transmit the waveform data from said memory to a computer through a transmission interface when the memory space of said memory used up (fully occupied), the step of driving said computer to write the received waveform data in a buffer thereof, and the step of running a test sample test signal auxiliary analyzing procedure for enabling the user to make data analyses based on the data received from said memory by said computer and displayed on a display screen of said computer.
2. The programmable logic analyzer data analyzing method as claimed in claim 1 wherein said test sample test signal auxiliary analyzing procedure includes a waveform quality analysis function.
3. The programmable logic analyzer data analyzing method as claimed in claim 1 wherein said test sample test signal auxiliary analyzing procedure includes a communication protocol analysis function.
4. The programmable logic analyzer data analyzing method as claimed in claim 1 wherein said test sample test signal

auxiliary analyzing procedure includes a memory data analysis function.

5. The programmable logic analyzer data analyzing method as claimed in claim 1 wherein when said control circuit  
5 fetched said waveform data from said test sample, a test sample data sheet inputted by the user is used for making the related analysis..

6. The programmable logic analyzer data analyzing method as claimed in claim 1 wherein when said control circuit  
10 fetched said waveform data from said test sample, the code number of the test sample selected from a database by the user is used for making the related analysis.

7. The programmable logic analyzer data analyzing method as claimed in claim 1 further comprising the step of storing  
15 analyzed data in the form of a file.

8. The programmable logic analyzer data analyzing method as claimed in claim 1 further comprising the step of printing out analyzed data through a printer.

9. The programmable logic analyzer data analyzing  
20 method as claimed in claim 1 wherein the capacity of the buffer of said computer varies with the amount of the internal data of said test sample..

10. The programmable logic analyzer data analyzing

method as claimed in claim 1 wherein said test sample test signal auxiliary analyzing procedure makes a debugging data analysis on the data fetched from said test sample.

11. The programmable logic analyzer data analyzing  
5 method as claimed in claim 1 wherein said test sample test signal auxiliary analyzing procedure makes a comparison data analysis on the data fetched from said test sample.

12. The programmable logic analyzer data analyzing  
method as claimed in claim 1 wherein said test sample test signal  
10 auxiliary analyzing procedure makes a search data analysis on the data fetched from said test sample.

13. The programmable logic analyzer data analyzing  
method as claimed in claim 1 further comprising the sub-step of  
using a compressor to compress the waveform data fetched by said  
15 control circuit from said test sample before driving said control  
circuit to store the fetched waveform data in said memory.

14. The programmable logic analyzer data analyzing  
method as claimed in claim 1 further comprising the sub-step of  
using a compressor to compress the storage waveform data for  
20 enabling compressed waveform data to be transmitted to said  
computer during the step of controlling said control circuit to  
transmit the waveform data from said memory to a computer  
through a transmission interface when the memory space of said

memory used up (fully occupied).

15. A programmable logic analyzer data analyzing method comprising the step of controlling a control circuit to fetch waveform data from the test sample and to store fetched waveform data in a memory, the step of writing the waveform data in a buffer when the memory space of said memory used up (fully occupied), the step of driving said control circuit to transmit the waveform data from said buffer to a display, and the step of running a test sample test signal auxiliary analyzing procedure for enabling the user to make data analyses based on the data received from said memory by said computer and displayed on a display screen of said computer.

16. The programmable logic analyzer data analyzing method as claimed in claim 15 wherein said test sample test signal auxiliary analyzing procedure includes a waveform quality analysis function.

17. The programmable logic analyzer data analyzing method as claimed in claim 15 wherein said test sample test signal auxiliary analyzing procedure includes a communication protocol analysis function.

18. The programmable logic analyzer data analyzing method as claimed in claim 15 wherein said test sample test signal auxiliary analyzing procedure includes a memory data analysis

function.

19. The programmable logic analyzer data analyzing method as claimed in claim 15 wherein when said control circuit fetched said waveform data from said test sample, a test sample 5 data sheet inputted by the user is used for making the related analysis..

20. The programmable logic analyzer data analyzing method as claimed in claim 15 wherein when said control circuit fetched said waveform data from said test sample, the code number 10 of the test sample selected from a database by the user is used for making the related analysis.

21. The programmable logic analyzer data analyzing method as claimed in claim 15 further comprising the step of storing analyzed data in the form of a file.

15 22. The programmable logic analyzer data analyzing method as claimed in claim 15 further comprising the step of printing out analyzed data through a printer.

23. The programmable logic analyzer data analyzing method as claimed in claim 15 wherein the capacity of said buffer 20 varies with the amount of the internal data of said test sample.

24. The programmable logic analyzer data analyzing method as claimed in claim 15 wherein said test sample test signal auxiliary analyzing procedure makes a debugging data analysis on

the data fetched from said test sample.

25. The programmable logic analyzer data analyzing method as claimed in claim 15 wherein said test sample test signal auxiliary analyzing procedure makes a comparison data analysis on  
5 the data fetched from said test sample.

26. The programmable logic analyzer data analyzing method as claimed in claim 15 wherein said test sample test signal auxiliary analyzing procedure makes a search data analysis on the data fetched from said test sample.

10 27. The programmable logic analyzer data analyzing method as claimed in claim 15 further comprising the sub-step of using a compression decompression device to compress said waveform data fetched from said test sample before storing in said memory and to decompress compressed storage waveform data  
15 before writing in said buffer after the memory capacity of said memory used up (fully occupied).

28. The programmable logic analyzer data analyzing method as claimed in claim 15 further comprising the sub-step of using a compression decompression device to compress said  
20 waveform data stored in said memory before writing in said buffer and to decompress the compressed waveform data before transmitting from said buffer to said display for display.